CLAIMS

What is claimed is:

1.   A   method   of   transmitting   parallel   data   to   a
destination   over   a   plurality   of   serial   data   lines,
comprising the steps of:

        segregating   the   parallel   data   into   a   plurality   of
parallel data words, each parallel data word comprising a
plurality of data bits;

        converting   the   plurality   of   parallel   data   words   to
respective serial representations of the data words;

        transmitting   the   respective   serial   representations
of the data words to the destination over the plurality
of serial data lines;

        transmitting a clock signal to the destination over
a   clock   line   in   parallel   with   the   plurality   of   serial
data lines, the clock signal having at least one data bit
of each parallel data word encoded thereon;

        converting the transmitted serial representations of
the   data   words   to   parallel   form   to   regenerate   the
plurality of parallel data words;

        aligning   the   regenerated   parallel   data   words   using
the respective data bits encoded on the clock signal; and

        regenerating   the   parallel   data   from   the   aligned
parallel data words.

2.   The method of claim 1 wherein the clock signal has a
predetermined clock rate, and the first transmitting step
comprises   transmitting   the   respective   serial

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representations of the data words over the plurality of serial data lines at the predetermined clock rate.

3. The method of claim 1 wherein the second transmitting step comprises transmitting the clock signal to the destination over the clock line, the clock signal having a single data bit of each parallel data word encoded thereon.

4. The method of claim 3 wherein the second transmitting step further includes transmitting the clock signal to the destination over the clock line, the clock signal having an edge density sufficient to allow recovery of the clock signal at the destination.

5. The method of claim 1 wherein the aligning step comprises converting at least a portion of the data bits encoded on the clock signal to parallel form to generate protocol data, selecting respective bit positions in each parallel data word and the protocol data, and comparing the data bits in the selected bit positions of the parallel data word and the protocol data to locate the at least one data bit of the parallel data word.

6. The method of claim 5 wherein the aligning step further includes aligning contiguous pairs of parallel data words based on the respective locations of the at least one data bit of the contiguous parallel data word pairs.

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7.   The method of claim 1 wherein the first transmitting step comprises transmitting the respective serial representations of the data words to the destination over the plurality of serial data lines at a serial data transmission rate of at least 2.5 GHz.

8.   A system for transmitting parallel data to a destination, comprising:

a protocol generator configured to (1) segregate the parallel data into a plurality of parallel data words, each parallel data word comprising a plurality of data bits, and (2) generate protocol data comprising at least one data bit of each parallel data word;

a plurality of parallel-to-serial converters configured to convert the plurality of parallel data words to respective serial data and convert the protocol data to a clock signal having the at least one data bit of each parallel data word encoded thereon;

a plurality of serial data lines configured to transmit the respective serial data to the destination;

a clock line configured to transmit the clock signal to the destination;

a plurality of serial-to-parallel converters configured to convert the respective serial data to parallel form to regenerate the plurality of parallel data words and convert at least a portion of the data encoded on the clock signal to parallel form to regenerate the protocol data; and

a de-skew circuit configured to (1) align the regenerated parallel data words using the at least one

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data bit of each parallel data word included in the protocol data, and (2) regenerate the parallel data from the aligned parallel data words.

5   9.   The system of claim 8 wherein the de-skew circuit is further configured to select respective bit positions in each parallel data word and the protocol data, and compare the data bits in the selected bit positions of the parallel data word and the protocol data to locate

10   the at least one data bit of the parallel data word.

10.   The system of claim 9 wherein the de-skew circuit is further configured to align contiguous pairs of parallel data words based on the respective locations of the at

15   least one data bit of the contiguous parallel data word pairs.

11.   The system of claim 8 wherein the plurality of parallel data words comprises a plurality of contiguous

20   pairs of parallel data words, and the plurality of serial data lines are configured to transmit serial data corresponding to the respective contiguous parallel data word pairs during successive time intervals.

25   12.   The system of claim 11 wherein the protocol generator is configured to segregate the parallel data into the plurality of parallel data words, each parallel data word comprising 8 data bits.

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13.   The system of claim 12 wherein each contiguous
parallel data word pair comprises a first parallel data
word and a second parallel data word, the first and
second parallel data words comprising respective upper
5   nibbles and respective lower nibbles, and wherein the
most significant bit of the upper nibble of the first
parallel data word and the most significant bit of the
lower nibble of the second parallel data word are encoded
on the clock signal.

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14.   The system of claim 13 wherein the clock signal has
an edge density sufficient to allow recovery of the clock
signal at the destination.

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